IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	M. Nandakumar et al	Examiner	Ortiz
Serial No.	09/876,292	Art Unit	2815
Filed	06/07/2001	Docket	TI-31089
For	ADDITIONAL N-TYPE LDD/POCKET IMPLANT FOR IMPROVING SHORT-CHANNEL NMOS ESD ROBUSTNESS		

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PETITION TO REVIVE

Sir:

Applicant hereby petitions the Commissioner to revive this application, on the grounds that abandonment was unintentional.

The application became abandoned on May 16, 2004 for failure to respond to the Notice of Drawing Inconsistency With Specification. A proper response to the Notice is enclosed herewith.

The required **fee of $1330.00** is also enclosed (check # 1314).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Gary C. Honeycutt, RegNo. 20250
Attorney for Applicant
972-470-0130
June 4, 2004

CERTIFICATE OF MAILING

It is hereby certified that this correspondence is being deposited with the United States Postal Service in an envelope bearing first class postage, addressed to Mail Stop Issue Fee, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on this the 4th day of June, 2004.

Gary C. Honeycutt

June 4, '04

06/08/2004 AWONDAF1 00000034 09876292
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09/876,292 UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

NOTICE OF DRAWING INCONSISTENCY WITH SPECIFICATION

The drawings filed 4/1/03 have been received. However, an inconsistency exists between the drawings and the Brief Description of the Drawings in the specification.

Figures _____ are listed in the Brief Description of the Drawings in the specification but not contained in the Drawings.

Figures 5-10 are contained in the Drawings but not listed in the Brief Description of the Drawings in the specification.

Applicant is required to correct the above-noted inconsistency within a time period of **ONE MONTH or THIRTY (30) DAYS, whichever is longer,** from the mailing date of this Notice, or within the time remaining in the time period set forth in the Notice of Allowability (Form PTOL-37) to file corrected drawings, whichever is longer. **NO EXTENSION OF THIS TIME PERIOD MAY BE GRANTED UNDER EITHER 37 CFR 1.136 (a) OR (b)**

Failure to correct the above noted inconsistency will result in **abandonment** of the application.

The file will be held in the Publishing Division to await the correction of the inconsistency.

Return Corrected Drawings/Specification to:
Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450

Alexandria, VA 22313-1450

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FORM PTO-1631 (REV. 10-03)

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AMENDMENT

Responsive to a Publishing Division requirement dated 04/16/2004 please amend the application as follows:

Page 8 of the specification, beginning at line 17, please add the following paragraph:

-- FIGS 5-10 are schematic cross sections illustrating the process flow for fabrication of a transistor in accordance with the invention. --

Remarks

This addition to the specification is a complete correction of the inconsistency.

A replacement page for the specification is enclosed.

Respectfully submitted,

Gary C. Honeycutt, RegNo. 20250
Attorney for Applicant
972-470-0130
June 4, 2004

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified and schematic cross section through a lateral MOS transistor, illustrating the current flow at an electrostatic discharge event.

FIG. 2 is a schematic plot of drain (collector) current, on a logarithmic scale, as a function of drain voltage, on a linear scale, illustrating the onset of the second breakdown phenomenon.

FIG. 3 schematically presents a cross section of a lateral MOS transistor with a photoresist window opened for the high energy ion implant according to the invention.

FIG. 4 illustrates schematically, yet in more detail, the cross section of the regions of the compensating ion implant of the invention.

FIGS 5-10 are schematic cross sections illustrating the process flow for fabrication of a transistor in accordance with the invention.

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